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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/918,604	07/30/2001	Haneef D. Mohammed	CYPR-CD01057	5237

7590 08/16/2004

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EXAMINER

DO, CHAT C

ART UNIT	PAPER NUMBER
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2124

DATE MAILED: 08/16/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

## Office Action Summary

### Application No.

09/918,604

### Applicant(s)

MOHAMMED ET AL.

### Examiner

Chat C. Do

### Art Unit

2124

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

### Status

- 1) ☒ Responsive to communication(s) filed on 30 July 2001.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

### Disposition of Claims

- 4) ☒ Claim(s) 1-19 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-19 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

### Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
  - ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

### Attachment(s)

- |   |   |
|---|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)   | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date: _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)                                    | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)             |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)<br>Paper No(s)/Mail Date: _____ | 6) <input type="checkbox"/> Other: _____  |

## DETAILED ACTION

### *Claim Objections*

1. Claims 17-18 are objected to because of the following informalities:

The applicant is advised to amend claims 17-18 to depend on the previous claim instead because they further define the limitations cited in the previous claim. Claim 17 should depend on claim 16 and claim 18 should depend on claim 17.

Appropriate correction is required.

### *Claim Rejections - 35 USC § 102*

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1-19 are rejected under 35 U.S.C. 102(e) as being anticipated by Kobayashi et al. (U.S. 6,199,091).

Re claim 1, Kobayashi et al. disclose in Figures 1-2 a method of performing a pipelined arithmetic function (wherein Figure 2 is an extension of Figure 1) comprising the steps of:

a) receiving two N-bit operands (e.g. X and Y are two N-bit operands) into each of a plurality of adder elements in separate pipelines (e.g. first adder yields Z0-Z2 and second adder yields Z3-Z8 in separate pipelines),

b) performing an add operation in each of plurality of adder elements wherein a first N-bit result (e.g. Z0-Z2) and a first carry bit (e.g. C1) is output from each of adder elements;

c) receiving first N-bit result from each of adder elements into a respective N-bit result register (e.g. registers to store the results for Z0-Z2) and receiving first carry bit from each of adder elements into a respective carry bit register (e.g. C1);

d) outputting from an incrementor (e.g. all the logics in the lower portion of producing Z3-Z4 except 7 and 9) in one of pipelines, a second N-bit result (e.g. Z3-Z4) and a second carry bit (e.g. C2) from the combination of a first result from a first of N-bit result registers (e.g. C1), a first carry bit from a first of carry bit registers (e.g. C1 from previous adder), and a first carry bit from a second of carry bit registers from a second of pipelines (e.g. second output line of 9); and

e) supplying a final result (e.g. Z3-Z8 for 9 bits) being a combination of second N-bit result from incrementor (e.g. C2 inputs into the next stage for computing Z5-Z8), second carry bit from incrementor, and first N-bit result (e.g. outputs of 13 and 17) from a second N-bit result register in second pipeline.

Re claim 2, Kobayashi et al. further disclose in Figures 1-2 the N-bit result registers are single width registers (e.g. non-register is double width).

Re claim 3, Kobayashi et al. further disclose in Figures 1-2 the carry bit registers are single bit registers (e.g. C1, C2, C3...).

Re claim 4, Kobayashi et al. further disclose in Figures 1-2 the step c) further comprises respectively receiving first N-bit result into a plurality of single width N-bit registers (e.g. box 7 it combines X3 and Y3 to yield a single bit result Z3).

Re claim 5, Kobayashi et al. further disclose in Figures 1-2 the step c) further comprises respectively receiving first carry bit into a plurality of single bit register (e.g. C1 is a single bit).

Re claim 6, Kobayashi et al. further disclose in Figures 1-2 the step d) further comprises respectively receiving second N-bit result into a plurality of single width N-bit registers (e.g. result of operands X,Y from 0-2 is Z0 to Z2).

Re claim 7, Kobayashi et al. further disclose in Figures 1-2 the step d) further comprises receiving second carry bit into a plurality of single bit registers (e.g. C2 is a single bit).

Re claim 8, it is an adder claim of claim 1 which has similar limitations. Thus, claim 8 is also rejected under the same rationale as cited in the rejection of rejected claim 1.

Re claim 9, it is an adder claim of claim 2 which has similar limitations. Thus, claim 9 is also rejected under the same rationale as cited in the rejection of rejected claim 2.

Re claim 10, it is an adder claim of claim 3 which has similar limitations. Thus, claim 10 is also rejected under the same rationale as cited in the rejection of rejected claim 3.

Re claim 11, it is an adder claim of claim 4 which has similar limitations. Thus, claim 11 is also rejected under the same rationale as cited in the rejection of rejected claim 4.

Re claim 12, it is an adder claim of claim 2 which has similar limitations. Thus, claim 12 is also rejected under the same rationale as cited in the rejection of rejected claim 2.

Re claim 13, it is an adder claim of claim 6 which has similar limitations. Thus, claim 13 is also rejected under the same rationale as cited in the rejection of rejected claim 6.

Re claim 14, it is an adder claim of claim 2 which has similar limitations. Thus, claim 14 is also rejected under the same rationale as cited in the rejection of rejected claim 2.

Re claim 15, Kobayashi et al. further disclose in Figures 1-2 a plurality of carry bit registers for respectively receiving carry bits from adder elements and incrementor (e.g. C1 from the first set of adder (1,3,5), C2 from the second set of adder(7,9) and incrementor (e.g. other lower portion of logics).

Re claim 16, it is a multistage adder claim of claim 1 which has similar limitations. Thus, claim 16 is also rejected under the same rationale as cited in the rejection of rejected claim 1.

Re claim 17, it is a multistage adder claim of claim 2 which has similar limitations. Thus, claim 17 is also rejected under the same rationale as cited in the rejection of rejected claim 2.

Re claim 18, it is a multistage adder claim of claim 6 which has similar limitations. Thus, claim 18 is also rejected under the same rationale as cited in the rejection of rejected claim 6.

Re claim 19, it is a multistage adder claim of claim 15 which has similar limitations. Thus, claim 19 is also rejected under the same rationale as cited in the rejection of rejected claim 15.

### ***Conclusion***

4. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

- a. U.S. Patent No. 5,619,441 to Bartling discloses a high speed dynamic binary incrementer.
- b. U.S. Patent No. 5,636,157 to Hesson et al. disclose a modular 64-bit integer adder.
- c. U.S. Patent No. 6,591,286 to Lu discloses a pipelined carry-lookahead generation for a fast incrementer.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chat C. Do whose telephone number is (703) 305-5655. The examiner can normally be reached on M => F from 7:00 AM to 4:30 PM.



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If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chaki Kakali can be reached on (703) 305-9662. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Chat C. Do  
Examiner  
Art Unit 2124

August 9, 2004

  
**KAKALI CHAKI**  
**SUPERVISORY PATENT EXAMINER**  
**TECHNOLOGY CENTER 2100**